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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NATNAEL, PAULOS M	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,141	KUEHN, HANS JUERGEN	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12,14 and 15* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **2-12,14,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Scheraga, U.S. Pat. No. **5,789,955**.

Considering claim **2**, a circuit arrangement as claimed in claim 1, characterized in that the amplification factor (n) is approximately 5.

Regarding claim 2, Scheraga discloses that the output current "...is multiplied by a factor referred to as beta, and appears at the collector current Ic that is caused to flow through the output load resistor, REXT". (see col. 5, lines 40-44) Scheraga however does not specifically give a number or a factor for amplification. Nevertheless, it would have been an obvious matter of design choice to modify the system of Scheraga (which does not disclose a specific amplification factor or number but nonetheless utilizes *some* amplification factor or number to amplify the signal) by providing an amplification factor of 5 or such other similar number, given the resulting expectation of similar desired output or effect of minimizing and reducing electromagnetic interference or

noise of the signal at the output of both the Scheraga reference and the claimed invention.

Considering claim **3,** a circuit arrangement as claimed in claim 1, characterized in that the signal is amplified in the pnp current mirror (16) or in the npn transistor current mirror (14), is met by the PNP current mirror circuit (fig.3). (see also col. 5, lines 15-20)

Considering claim **4**, a circuit arrangement as claimed in claim 1, characterized in that the high voltage source (30) supplies a voltage of the order of approximately 12 V, is met by the VBAT 12V output voltage source, Fig.3.

Considering claim **5**, a circuit arrangement as claimed in any one of claim 1, characterized in that the input (12) ...is preceded by at least one supply or driver circuit (40) by which the low current (I) input signal can be applied to the adapter circuit (10), is met by voltage supply VCC (5.0V) and R3, fig.3;

Considering claim **6**, a circuit arrangement, as claimed in claim 5, characterized in that the supply or driver circuit (40) is connected to at least one low voltage source (42).

Regarding claim 6, see rejection of claim 5.

Considering claim **7**, a circuit arrangement as claimed in claim 6, characterized in that the low voltage source (42) supplies a voltage of the order of approximately 1 V to approximately 3.3V;

Regarding claim 7, Scheraga discloses 5 Vcc supply as the low voltage source for the input of the device. However, it would have been an obvious matter of design choice to modify the system of Scheraga by providing a lower voltage source between approximately 1 V to 3.3 V, since applicant has not disclosed that having such range of low voltage solves any stated problem or is for any particular purpose and it appears that a similar voltage would perform equally well.

Considering claim **8**, Scheraga discloses the following claimed subject matter, note;
a) the npn transistor arrangement (14) is constituted as an npn current mirror and/or particularly as an NMOS current mirror (NMOS = N-channel Metal Oxide Semiconductor = N-channel Metal Oxide Semiconductor), is met by the NPN current mirror circuit, fig.3;

b) the pnp transistor arrangement (16) is constituted as a pnp current mirror and/or particularly as a PMOS current mirror (PMOS = P-channel Metal Oxide Semiconductor = P-type Metal Oxide Semiconductor), is met by the PNP current mirror circuit, fig.3.

Considering claim **9**, a circuit arrangement characterized in that the output (18) of the adapter circuit (10) precedes at least a resistor (50) for converting the higher current (Io) output signal into a higher voltage (Uo) output signal;

Regarding claim 9, Scheraga discloses an external Resistor (Rext). However, doesn't disclose a resistor at the output 18 in order convert the current into voltage. Nevertheless, the examiner takes Official Notice in that it is notoriously well known in

the electronic art to utilize resistor(s) connected from the output to ground to convert the output current into output voltage and, therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Scheraga by providing a resistor in order to be able to determine the output voltage of the circuit so that it would be used to drive the next stage.

Considering claim **10**, the claimed a circuit arrangement as claimed in claim 9, characterized in that the resistor (50) has a value of approximately 1 K ohms.

Regarding claim 10, Scheraga does not discloses a resistor at the output 18; However, as shown above in claim 9, it is notoriously well known to employ a resistor to convert current to output voltage by utilizing a resistor, and therefore, it would be an obvious matter of design choice to select a value of the resistance according to the desired output value or level and modify the system of Scheraga accordingly.

Considering claim **11**, a circuit arrangement as claimed in claim 1, characterized in that the output (18) of the adapter circuit (10) precedes at least a SCART (= Syndicat des Constructeurs d'Appareils Radii Receteurs et Televiscurs) output (70).

Regarding claim 11, Scheraga does not specifically disclose a SCART socket. However, the Examiner takes Official Notice here in that the SCART socket is well known in the art for use in input and/or output terminals of circuits such as amplifiers and, thus, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Scheraga by providing a SCART socket at the output

of the amplifier so that the system would be able to determine or check what sort of signal is being transmitted from current mirror stage to the next stage and thus have control of the transmitted signals.

Considering claim **12**, a circuit arrangement wherein the circuit is multi-staged is met by input stage, the pnp current mirror stage, and the npn current mirror stage, and the output stage (fig.3). (Note: Since the claim is recited in the alternative, the examiner is meeting the first part in the and/or alternative).

Considering claim **14**, a television, multimedia, radio or video recording device comprising at least a circuit arrangement (100) as claimed in claim 15.

Regarding claim 14, see rejection of claim **15**.

Considering claim **15,** Scheraga discloses all claimed subject matter, note;
a) a circuit arrangement, comprising: at least one adapter circuit (10), which amplifies an analog input signal of a low current (Ii) by an amplification factor (n) into a particularly analog output signal of a higher current (Io),

is met by the circuit arrangement utilized in radio or television illustrated in Fig.3 which has an input voltage of 5V Vcc and the output voltage is connected/assigned to the VBAT 12V and whose input current is approximately 0.2mA and has an output current that "...is multiplied by a factor referred to as beta, and appears at the collector current

Ic that is caused to flow through the output load resistor, REXT". (see col. 5, lines 40-44)

b) the claimed "an input (12) which corresponds to the range of low voltage (U)," is met by the 5 Vcc, Fig.3, which is connected to the input stage.

c) the claimed, "an output (18) which corresponds the range of higher voltage (Uo)", is met by the high voltage source 12V, fig. 3, that is connected to the output stage.

d) the claimed, comprises at least one npn transistor current mirror (14), is met by npn transistor current mirror circuit, fig.3.

e) the claimed, at least one pnp current mirror (16) arranged in series with the npn transistor current mirror (14) and connected to at least one high voltage source (30), is met by the pnp current mirror circuit (fig. 3), which is connected to voltage source VBAT 12V, fig.3 and that "an NPN transistor current mirror and a PNP current mirror [are] connected in series". (see Abstract)

Except for;

f) the claimed <u>wherein the at least one pnp transistor current mirror amplifies the input signal, which is received from the at least one npn transistor current mirror</u>;

Regarding the newly added limitation (f), Scheraga does not specifically use the word "amplification" or "amplifying" with regard to the pnp current mirror circuit. However, Scheraga does not preclude such a function. In fact, Scheraga teaches

current multiplication, i.e., amplification, at the output of the circuit compared to the input, thusly: "a current mirror is a circuit, known in the art, which has an input port, an output port, and a common port. The current flowing between the common port and the output port is a specified multiple of the current between the common port and an input port. The specified ratio of output current to input current is determined by the design of the current mirror. Thus, with no current flowing out of PNP CURRENT SPLITTER, NPN CURRENT MIRROR has no input current, and, consequently, provides no output current." [emphasis added by examiner] Col. 3, lines 25-34 Even though, Scheraga does not use the term "amplification" or "amplify" with regard to the pnp current mirror circuit, it would have been obvious to the skilled in the art to readily recognize the teaching of Scheraga as such and implement the system accordingly.

Response to Arguments

3. Applicant's arguments filed 11/8/04 have been fully considered but they are not persuasive. Applicant argues that the Scheraga does not disclose the use of a pnp current mirror to amplify an input signal from an npn transistor current mirror.

The Examiner submits, as shown in the rejection above, that Scheraga teaches there is indeed amplification occurring when disclosing the current flowing between the common port and the output port is a specified **multiple** of the current between the common port and an input port. This, given a reasonably broad interpretation, is a form amplification, albeit not explained very well in the Scheraga reference. The argument is therefore unpersuasive.

Allowable Subject Matter

4. Claim **13** is again objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art, Scheraga, fails to disclose a circuit arrangement wherein eight npn transistors and 24 pnp transistors are provided and in that a four-stage adapter circuit or four adapter stages precede a resistor, as in claim **13**;

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571)272-7353. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
May 13, 2005

PAULOS M. NATNAEL
PATENT EXAMINER